Short Keynote: Embedded Fault-Tolerant Architecture for Synthetic-Aperture Radar Backprojection

***Abstract*—This paper presents an optimized multicore embedded architecture to speed up and improve the resilience of the execution of a backprojection algorithm targeting onboard Synthetic-Aperture Radar (SAR) imaging systems for the space environment. The proposed architecture produces SAR images by computing approximations instead of the full precision of some arithmetic operations. The proposed solution was implemented on a Xilinx SoC device with a dual-core processor. The novel fault-tolerant system exhibits graceful degradation characteristics as it is able to produce images considered acceptable, that is, with an Signal-To-Noise Ratio (SNR) value above 100 dB and on average with an SNR 0.65 dB less than the fault-free image, while providing a time reduction up to 33%, and a decrease up to 40% in energy consumption.**

I. Summary

Synthetic Aperture Radar has been heavily used for Earth observation. SAR is an enticing method for monitorization because it does not require a light source, being capable of operating even under adverse weather conditions and at night time. Several observation missions, including ESA Sentinel and Envisat, Alos Palsar, TerraSAR-X, Cosmo-SkyMed and Radarsat are being used to monitor ice caps, land, oceans, vegetation, sea-surface topography and natural disasters such as hurricanes, volcano eruptions and earthquakes [1]. Due to the effects of radiation, space is a severe environment for digital electronic systems. For this reason, on-board systems must be reliable and tolerate radiation-induced errors.

SAR systems are challenging to design since they require the implementation of computationally intensive algorithms. Typically, the acquired data is processed off-board, leading to the transmission of large quantities of data, hence it is of great interest to have high-performance embedded onboard systems capable of implementing such algorithms and broadcasting SAR images, while being fault-tolerant.

Backprojection (BP) is an algorithm for SAR image generation capable of generating high quality images. BP is considered the reference algorithm for SAR due to its ability to generate images with higher quality when compared to other algorithms. The main drawback of the algorithm is its high computational cost, with a complexity of $O(n^3)$.

Fault-tolerant systems are capable of detecting and correcting faults that may occur. Precise fault-tolerant mechanisms rely on repetitions of the same operation, followed by a comparison of the obtained results in order to assess the most common, which is assumed to be the correct value. Previous work on implementations of fault-tolerant SAR image generation algorithms is presented in [2], [3], [4]. A fault-management unit responsible for periodically scrubbing the FPGA configuration data, test a fault condition, remove a faulty processor from the circuit and replace it by an alternative processor, and a Triple Modular Redundancy (TMR) mechanism is used in the execution of a SAR algorithm are used in [2]. Concurrent Error Detection (CED) for the Fast-Fourier Transformer (FFT) algorithm is used in [3], [4]. Besides CED, [3] also implements weighted sum and FPGA scrubbing.

Since the Backprojection algorithm is, by itself, a computationally intensive algorithm, the objective was to develop a fault tolerance mechanism with a reduced overhead in the system compared to traditional mechanisms. As mentioned, the algorithm generates images with higher quality than the other image formation algorithms. For this reason, small deviations due to faults may be imperceptible in the resulting image. Extensive work in this research area is devoted to the trade-off between the accuracy of the results and efficiency. Often, the proposed methods rely on the computation of truncated or approximate functions and Look-Up Tables (LUTs) [5].

The focus of this keynote is the fault tolerance mechanism developed specifically for the Backprojection algorithm, which results from a modification to the TMR mechanism, where only two calculations are executed, combined with approximate computing, allowing a small quality loss in trade for efficiency.

References

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