Guest Editors' Introduction

SBCCI 2022

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The Symposium on ICs and Systems Design (SBCCI) is an international forum dedicated to ICs and systems design, test, and EDA, held annually in Brazil. Over the past four decades, SBCCI has established itself as an important international forum for the presentation of research results on leading-edge aspects of ICs and systems, such as analog circuits, mixed-signal and digital ICs design, dedicated and reconfigurable architectures, EDA tools, design methods, embedded systems, SoC, and nanoarchitectures, as well as verification and test methods. This 35th edition of SBCCI was held virtually, on the metaverse, but the organization was centered in Rio Grande do Sul state, Brazil. This gave origin to the name Chip in the Minuano.

This special issue contains extended versions of the best papers presented at SBCCI 2022. These papers have been again refereed along the usual refereeing process in force at *IEEE Design&Test*. We are proud to offer these papers to the readers of *IEEE Design&Test*. Five papers, covering a variety of topics related to the event, have been finally selected, as follows.

- "Integrating Machine-Learning Probes in FPGA CAD: Why and How?" [A1] discusses challenges posed by current designs and proposes the adoption of machine-learning probes in the FPGA design flow to improve performance.
- "Flexible and Scalable BLAKE/BLAKE2 Coprocessor for Blockchain-Based IoT Applications" [A2] proposes a flexible and scalable BLAKE/BLAKE2 coprocessor aiming for high flexibility, high performance, and low power for blockchain-based Internet of Things (IoT) applications.
- "Heuristic-Based Algorithms for Low-Complexity AV1 Intra Prediction" [A3] presents a fast mode decision scheme and a mode-adaptive subsampling algorithm to accelerate AV1 encoding.
- "Seamless Thermal Optimization of Parallel Workloads" [A4] proposes a framework for thread-throttling and core-frequency optimization. The framework titled TAURUS is dynamic and transparent to the end user.
- "SeMAP—A Method to Secure the Communication in NoC-Based Many-Cores" [A5] presents a method for the secure execution of applications on multiple-processors SoCs (MPSoCs) by adopting spatial isolation of applications and a secure communication mechanism with peripherals.

We hope you enjoy these contributions as much as we did. ■

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Appendix: Related Articles

[A1] T. Martin et al., "Integrating machine-learning probes in FPGA CAD: Why and how?" *IEEE Des. Test*, vol. 40, no. 5, pp. 7–14, Sep. 2023.

[A2] H. L. Pham et al., "Flexible and scalable BLAKE/BLAKE2 coprocessor for blockchain-based IoT applications," *IEEE Des. Test*, vol. 40, no. 5, pp. 15–25, Sep. 2023.
[A3] M. Corrêa et al., "Heuristic-based algorithms for low-complexity AV1 intra prediction," *IEEE Des. Test*, vol. 40, no. 5, pp. 26–33, Sep. 2023.
[A4] S. M. V. N. Marques et al., "Seamless thermal optimization of parallel workloads," *IEEE Des. Test*, vol. 40, no. 5, pp. 34–41, Sep. 2023.
[A5] R. F. Faccenda et al., "SeMAP—A method to secure the communication in NoC-based many-cores," *IEEE Des. Test*, vol. 40, no. 5, pp. 42–51, Sep. 2023.

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