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EDITORIAL

Special issue on real-time energy-aware circuits and systems for HEVC and for its 3D and SVC extensions

Leonel Sousa[1] · **Nuno Roma**[1]

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Since its approval, in 2013, the high-efficiency video coding (HEVC) standard [1, 2] has established as the new state-of-the-art on video compression. When compared with the previous standards, it has been shown that HEVC encoders can achieve equivalent subjective visual quality as their predecessor H.264/AVC encoders, when using approximately 50% less of the bit rate [3–5]. However, such coding efficiency comes at the cost of a substantial increase in the computational complexity of the video codec [6, 7]. As a consequence, the implementation of real-time HEVC codecs is still an open and challenging task, only attained by highly optimized algorithms allied with very efficient processing circuits and streaming techniques [8].

Complementarily, with the recent advent of its standardized extensions—i.e., range extensions (REext) [9], scalable high efficiency video coding (SHVC) [10], multiview high efficiency video coding (MV-HEVC) and 3D high efficiency video coding (3D-HEVC) [11])—added support for: (1) more color formats (4:0:0, 4:2:2 and 4:4:4) and bit depths higher than 10 bits; (2) spatial and fidelity scalability; and (3) multiview and 3D-video coding [12] has been included in HEVC. As a consequence, the pressure for the development of convenient high-throughput and real-time encoding/decoding systems and supporting hardware structures has gained a renewed interest by the research community.

✉ Leonel Sousa
leonel.sousa@inesc-id.pt

Nuno Roma
nuno.roma@inesc-id.pt

[1] INESC-ID, Instituto Superior Técnico, Universidade de Lisboa, Rua Alves Redol, 9, 1000-029 Lisbon, Portugal

However, although conventional approaches (often relying on programmable and/or dedicated parallel processing platforms) already allow achieving significant performance levels [13], important compromises have to be established in order to cope with the strict energy efficiency requirements imposed at the several different application domains (e.g. mobile, battery supplied and hand-held devices). As a consequence, energy efficiency is gradually becoming a fundamental constraint and requisite for video encoding/decoding systems design, often requiring the adoption of new technologies and micro-architecture design approaches.

This special issue (SI) of the Springer Journal of Real-Time Image Processing (JRTIP) entitled "Real-Time Energy-Aware Circuits and Systems for HEVC and for its 3D and SVC Extensions" is mainly focused on the new design and development trends of energy efficient and real-time processing architectures for HEVC systems. The collection of papers presented here emphasizes several aspects of this research domain, including not only architectures but also algorithms and circuits.

The call for papers resulted in 11 submissions. For each submission, at least two reviewers examined its quality, together with the guest editors and the editors-in-chief. Finally, six papers were selected, which can be grouped into two main different topics. One involves architectures and low-power optimizations for energy efficient implementations of real-time HEVC coding systems. The other topic is focused on the 3D/SVC HEVC extensions, comprising several techniques for real-time energy-aware implementations of these technologies.

The paper entitled *Complexity Control of HEVC Encoders Targeting Real-Time Constraints*, by Mateus Grellert, Bruno Zatt, Muhammad Shafique, Sergio Bampi, and Jörg Henkel, proposes an adaptive complexity control scheme to

dynamically adjust the encoder to the varying computing capabilities of the hardware platform. For such purpose, an extensive complexity analysis of key HEVC encoding parameters was presented, making use of a new parameterized complexity model denoted by "Arithmetic Complexity". The presented results show that the proposed scheme provides time savings ranging from 10% up to 90%, with an average error (between the target and the effective complexity) of 1.2%. Their adaptability and control performance analysis also shows that this scheme rapidly adapts to dynamic set-point adjustments. Compared to the state-of-the-art, the presented complexity control achieves more accurate results and extra features (such as dynamic set point adjustment) at the cost of minor losses in coding efficiency.

The paper on *Architecture-Aware Optimization of an HEVC decoder on Asymmetric Multicore Processors*, by Rafael Rodríguez-Sánchez, and Enrique S. Quintana-Ortí, considered the usage of low-power asymmetric multicore processors (e.g. ARM big.LITTLE) to implement an HEVC decoder, in order to exploit their performance-power ratio for energy-constrained environments. In particular, considering that these processors integrate cores with different performance capabilities, these authors analyzed asymmetry-aware scheduling solutions to distribute the workload among the several processors. The performance and energy efficiency of the presented solution was further enhanced by exploiting the NEON vector engine available in the ARM big.LITTLE architecture. The presented evaluation, conducted on a Samsung Exynos 5422 system-on-chip (ODROID-XU3 board) equipped with an ARM big.LITTLE processor, exposed a 1080p real-time HEVC decoding capability at 24 frames/sec and a reduction of energy consumption over 20%.

The paper entitled *Efficient DVFS for Low Power HEVC Software Decoder*, by Erwan Nogues, Julien Heulot, Glenn Herrou, Ladislas Robin, Maxime Pelcat, Daniel Menard, Erwan Raffin, and Wassim Hamidouche, presents a low power HEVC software decoder that exploits dynamic voltage frequency scaling (DVFS) and dynamic power management (DPM) techniques made available in the latest ARM big.LITTLE system-on-a-chip (SoC) processors to increase the processing efficiency and reduce the energy consumption. Two approaches were presented: boosted DVFS (BDVFS), which aims minimizing the decoding latency by preventing any deadline miss throughout the decoded sequence; and adaptive DVFS (ADVFS), which adapts its processing frequency in a quasi pro-active fashion, before decoding the current frame. The resulting implementation was thoroughly evaluated both with power efficiency and real-time metrics (e.g. deadline-miss-ratio and latency) and compared both to standard Linux governors and state-of-the-art DVFS management techniques, achieving power savings close to the upper bound that DVFS can achieve.

The paper on *Energy-Aware Scheme for the 3D-HEVC Depth Maps Prediction*, by Mário Saldanha, Gustavo Sanchez, Bruno Zatt, Marcelo Porto, and Luciano Agostini, presents an energy-aware scheme to reduce the energy consumption on the 3D-HEVC depth maps prediction mode based on a qualitative evaluation of the depth maps characteristics. Both intra and inter-frame predictions were considered in this evaluation. Likewise, the use of the diamond search (DS), one at a time search (OTS), and small diamond search pattern (SDSP) was analyzed to substitute the test zone search (TZS) for depth maps, aiming to simplify the inter-prediction procedure. According to the authors, these three algorithms can lead to different complexity, energy and video quality operation points. As a result, they can be integrated into the encoder, which will adaptively choose the best algorithm according to the application requirements. When combined with the simplified edge detector (SED) algorithm, they are capable of significantly reducing the complexity and energy (21.2–23.1 and 9.85–10.41%, respectively) with minimum quality losses.

The paper entitled *Real-Time Scalable Hardware Architecture for 3D-HEVC Bipartition Modes*, by Gustavo Sanchez, César Marcon, and Luciano Agostini, presents a real-time scalable hardware architecture for the bipartition modes of the 3D-HEVC standard extension, which includes the depth modeling modes 1 (DMM-1) and 4 (DMM-4). In particular, a simplification of the DMM-1 algorithm was presented, by removing its refinement step. This simplification causes a small Bøntegaard Delta rate (BD-rate) increase (0.09%) with the advantage of better using the hardware resources, reducing by 30% the amount of memory required to store all DMM-1 wedgelet patterns. This scalable architecture can be configured to support all the different block sizes supported by the 3D-HEVC, and also to reach different throughputs according to the application requirements. The presented synthesis results show that the designed architecture is capable of processing HD 1080p videos in real-time, but higher resolutions are also possible to be processed with other configurations of the architecture.

The paper on *Optimization of Depth Modeling Modes in 3D-HEVC Depth Intra Coding*, by Yuhua Zhang, Yong Wang, Ce Zhu, Yongbing Lin, and Jianhua Zheng, presents three new approaches to accurately and efficiently predict the constant partition value (CPV) of each depth block region. A better CPV predictor was obtained by simply extending the actual depth map boundary, which can also simplify the CPV prediction by removing comparisons and average operations. Furthermore, the authors propose to choose an optimal combination of delta CPVs in terms of

view synthesis optimization (VSO) at the encoder by checking more candidates. Finally, zero residual coding is suggested for depth modeling modes (DMMs) coding units in the rate-distortion optimization loop. The experimental results demonstrate that, on average, about 0.2 and 0.1% BD-rate saving can be achieved for synthesized views with less complexity, under the all-intra (AI) and random access (RA) configurations, respectively.

To conclude, the guest editors would like to thank the authors and the reviewers for their contribution and support for this special issue. We are confident that the presented set of proposals represents relevant steps to help the community to continue pursuing the challenging task of coping with the demanding computational requisites that are required to attain real-time implementations of HEVC codecs, while still being able to cope with the strict energy efficiency requirements that are imposed at the several different application domains.

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