Co-Simulation for the Evaluation of IEC 61850 based Protection Schemes

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***Abstract*—The paper describes a dedicated co-simulation architecture to combine power system (PS) simulation and information and communications technology (ICT) simulation, to assess new protection schemes fully compliant with the IEC 61850 standard. The interaction between the two simulators has been validated by an example showing the generated Ethernet traffic by a simple substation protection scheme under a power system fault condition. Simulation results are presented from the power system perspective, by means of voltage and current oscillography and from the ICT system perspective, using an especially developed sequence diagram of the transferred Ethernet messages. By using the proposed architecture, the time performance of protection schemes based on process bus can be assessed.**

***Index Terms*-- Power system simulation, ICT simulation, co-simulation, protection system, IEC 61850.**

I. Introduction

Protection schemes are complex systems used to detect disturbances in the power grid and isolate, by means of circuit breaker tripping, sections of the power grid that are required to clear the disturbance, bringing back the power grid to normal operation. The new protection schemes are designed to fully support the IEC 61850 communication standard [1], which comprehends the combined use of intelligent electronic devices (IED) and local area networks (LAN). Two LAN networks are employed by protection schemes. The first, named station bus, is used for alarming, signaling and maintenance; the second, named process bus, is used for the most critical functions such as electric quantities measurement, tripping and blocking. While station bus LANs have been deployed by utilities during the last years, process bus LANs only now are being designed and the first protection schemes being deployed.

Beyond the traditional considerations used during the design of protection schemes, the design of the new schemes must address the station and process bus networks, in accordance with the communication system requirements part of the IEC 61850 standard. These requirements include component failure conditions, redundancy design, recovery times and message transfer time. As the protection schemes performance is dependent on the LAN performance, the design process requires the combination of different studies, which may include simulation and real time testing by using the system in the loop (SITL) techniques [2-10].

Although SITL tests are the most reliable type of tests, they present scalability limitations as the cost and time required for assembling physical devices and testing large systems may become prohibitive. Notwithstanding the need for real time testing, preliminary steps in the design process of such systems are made using simulation.

Simulating the operation of protection schemes may either be achieved by using a given simulation environment [6-7] (integrated simulation) or by splitting into different environments [11-14, 22-24] using a joint and synchronized simulation (co-simulation).

Integrated simulation has the advantage that all system components are modelled in one single simulation environment, the Power System (PS) simulator or the Information and Communications Technology (ICT) simulator. The choice depends on the aim of the study. In case the study aims at assessing the protection scheme interaction with the PS it is likely to choose the PS simulator. On the other hand, if it aims at assessing the performance of the ICT network, the ICT simulator shall be used. In either case, a high degree of abstraction is typically adopted in the models that are not native to the simulation environment and, eventually, limiting the representativeness of reality. Complex models can be developed in the simulation environment, but this process is costly and not always feasible.

Co-simulation benefits from using the most appropriate models and solvers from different simulation environments and, therefore, reducing the cost and time required to model development and validation. In a co-simulation environment, the reality is usually split between simulators respecting the natural frontiers between different physical domains. During a co-simulation, the data exchanged between simulators is restricted to discrete simulation time instants, as each simulator runs independently, except for these synchronization instants. A common server provides a set of general purpose services to support the interaction between simulators and their time synchronization.

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Important standards exist for co-simulation aiming to provide a standard interface for coupling different simulators under the same co-simulation environment. The most widely supported is the High-Level Architecture (HLA) and one such system for co-simulating PS and ICT networks is described by Georg et. al. [11]. Extensive overviews of various power systems and communication network co-simulation implementations have been published by Mets et al. [12] and by Levesque et. al [13]. Mostly, the applications are concerned with wide-area monitoring, protection, control and demand side response.

A thoughtful approach to design process bus networks has been made by the authors by using integrated simulation [15], where basic models of the PS IEDs were developed in the ICT simulator, capable of reproducing a sequence of events and equipment states under different operation scenarios, including normal operation and power system fault disturbances. The simulation was used for assessing the functional correctness of steady-state operation of the protection scheme, as well as during a power system fault clearance process.

The co-simulation environment, especially developed here to assess protection schemes that acquire sample values measurements and publish/subscribe Generic Object Oriented Substation Events (GOOSE) message commands through a process bus LAN, does not follow the HLA [16-18] or Functional Mock-up Interface (FMI) [19] standards, but follows the same architecture. The next section defines the co-simulation architecture developed for the project, using OPAL-RT HYPERSIM as the PS simulator and Riverbed Modeler as the ICT simulator.

Experiments showed that it is not possible to control the simulation progress when executing a simulation in real-time mode. In real-time mode, each process is advanced based on an external clock reference, such as IEEE 1588 signal, and not from an external co-simulation server. Therefore, all co-simulations were executed in off-line mode. Each process in the HYPERSIM simulator is now controlled and synchronized at the end of each 50μs time step. Data is exchanged between simulators at a lower rate using 1 ms intervals.

This paper demonstrates how two best-of-the-breed simulators in their respective fields can be connected to accurately simulate the effects of the communication network architecture on the operation of substations.

The remainder of the paper is as follows. The co-simulation architecture is described in Section II. Sections III-V describe the implementation of the architecture in the used simulators. A substation scenario is simulated in Section VI and conclusions are drawn in Section VII.

II. Co-Simulation Architecture

The Power System and ICT simulations are controlled and synchronized by means of a Co-simulation Coordinator Server, specially developed for this purpose. The coordinator launches the Power System and ICT simulations, controlling the simulation time, collecting and storing the simulation outputs for post-simulation analysis.

In each simulator, one simulation interface manages all data transferred between simulators, sending to the Co-simulator Coordinator Server the simulation data of interest for post-simulation analysis. Additionally, one simulator controller in the power system simulator is used to start/stop the simulation of power system disturbances.

Simulating the operation of IEC 61850 protection schemes and the supporting process bus network requires the simultaneous simulation and interaction between three domains: the PS, the ICT and the IED, presented in Figure 1.

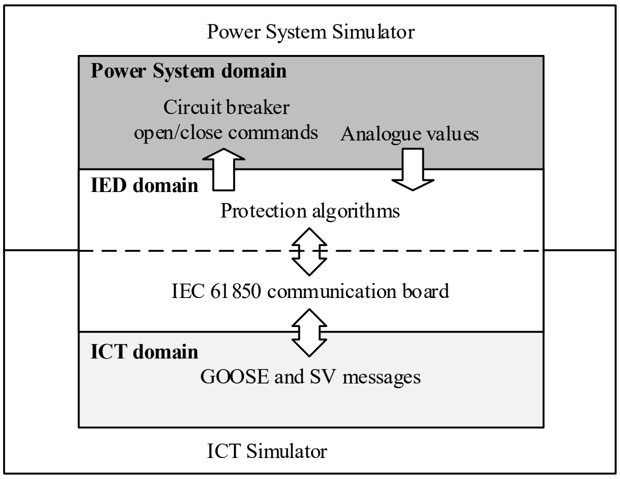

Figure 1. Interactions between the Power System, ICT and IED domains.

The Power System Simulator simulates the power system domain considering all power system elements and the grid topology, including substation arrangement comprising circuit breakers, disconnect switches and instrument transformers.

The ICT simulator simulates the process bus network considering how IEDs are interconnected through the Ethernet communication infrastructure, and how traffic flows are treated inside the network, including the implementation of the Ethernet protocol, the IEC 61850 communication interface requirements, the dimensioning of switches, number of ports and speed of the links.

As regards the IED domain, it represents the electronic devices comprising the protection algorithms and the Ethernet communication interface, including the implementation of the IEC 61850 communication requirements. Since this domain interacts with both the Power system and ICT domains, its model and simulation is split between the ICT and the Power system simulators

In this work, the OPAL/HYPERSIM [20] software was chosen to simulate the power system domain, as it allows simulating in the time domain complex power systems, includes customized C code for external interface with other simulators and can be controlled from an external server. The Riverbed/MODELER [21] software was chosen to simulate the ICT domain, as it benefits from the External Simulation Access (ESA) API package for exchanging data values with external simulators and includes customized C code for control from an external server.

III. IED model

The IED model considers the existence of a processor board and a communication board inside the IED. Accordingly, the IED processor board is modeled in the power system simulator while the Communication board is modeled in the ICT simulator, Figure 2.

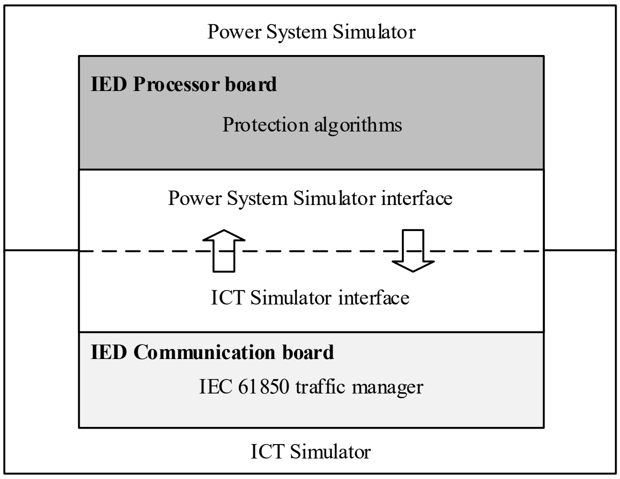

Figure 2. Split modeling of IED domain between Power System and ICT simulators.

A. Processor board

The IED Processor board comprehends all the protection algorithms and the corresponding interface with the IED Communication board. The protection algorithms encompass analog measurement, signal processing, binary I/O signals interface from the power system, binary I/O signals interface from the simulator interface and tripping criteria. There is no limitation in the level of detail used in modelling the protection algorithms, this being dependent only on the study requirements.

The Power System Simulator interface maps the protection algorithms' binary I/O signals to the subscribed/published GOOSE message payloads. In case the GOOSE message payload changes, the interface sends to the IED Communication board the new GOOSE message to be published in the process bus network.

A power system simulator library was especially developed for the simulator interface. This library is responsible for the communication with the co-simulation coordinator, as well as with each IED model within the Power System simulator. Additionally, it is in charge of controlling the simulation time.

The time delay consumed by the IED Processor board is modeled using a uniform random process delay between 1 ms and 1.2 ms, based on the recommendation from IEC 61850. Accordingly, it corresponds to the scheduled time of each GOOSE message delivery to the IED Ethernet physical port, i.e. after the IEC Communication board.

B. Communication board

The IED Communication board comprehends the IED 61850 traffic manager, which encompasses GOOSE and Sampled Value (SV) traffic publish/subscribe and interpreter.

Given its purpose, different GOOSE message types exist in a substation, each having a specific content and according to the developed engineering design.

GOOSE message publishing respects the IEC 61850 requirements. Accordingly, messages are published at a constant rate, the heartbeat T0, e.g., 5s, and a stream of GOOSE messages is published after any change in the message payload data. In this case, the IED Communication board publishes immediately a new GOOSE message with the new payload value and changes the publish interval to T1, e.g., 2 ms. After publishing two repetition messages, the publish interval is changed to T2, e.g., 4 ms. After publishing another message, the publish interval is changed to T3, e.g., 8 ms. After publishing a final message, the publish interval is changed back to T0, and the steady state is reached again. It should be noticed that considering the previous time intervals, during an event (T1 interval), traffic increases 2500x above the steady state rate. About 16 ms (2*T1+T2+T3) after an event, the steady state is reached again.

In order not to transmit duplicated data from the IED communication board to the IED Processor board, each receiving IED in the ICT simulator filters out only those messages that have a different payload than the previously received message from the same publisher. This greatly reduces the number of messages to be passed around between simulators, and hence, speeds up the simulation, without altering its outcome.

The process time for GOOSE subscription is included in the IED Communication board interface by scheduling each GOOSE message delivery time to the Protection Algorithms in the IEC Process board.

During the simulation, the different IEDs are considered to be unsynchronized, meaning that they all start publishing messages at some random time and not all at the same instant. In order to take into account any error in clock synchronization between IEDs along the network, some randomness is added through a Gaussian distribution (with zero average and standard deviation of 2 μs) applied to each T0 interval, whose probability density function is:

$$f(x) = \frac{1}{\sqrt{2\pi \times 2^2}} e^{\left(-\frac{x^2}{2\times 2^2}\right)} \tag{1}$$

where x is the time (in μs, positive or negative) that is added to T0.

In the ICT simulator, each GOOSE message packet sent between IEDs via the modeled process bus network, or between the logical and communication part of the nodes, has a value of the INT-type with a width of 32 bits. The highest 8 bits of the INT are used to store the message identifier, e.g., the encoded name of the publisher IED. The remaining 24 bits contain data, with a specified format for each message type. As an example, the GOOSE message used to operate a circuit breaker contains 8 bits of data, which are Double Point (DP) indications of which phases should be tripped or closed, with one bit pair associated with each of the three phases and another bit pair used when the command is issued to the three phases at the same time. Each bit pair contains one of the following command codes: Trip (01) or Close (10). The other values are reserved for future use. If the message intends to trip phase three only, the message content will be the following: 00 00 01 00.

In the Power System simulator, an especially developed block is used on each IED to map the corresponding published and received GOOSE messages to internal logical variables used by the protection algorithms.

Further to GOOSE messages, the IED communication board also publishes/subscribes SV messages. The SV message is a type of message used by the protection scheme to transmit analog current and voltage measurements. The IEC 61869-9 standard [26] standardizes the digital interface for instrument transformers. This introduces the FfSsIiUu notation for the SV stream, where: f is the digital output sample rate expressed in samples per second; s is the number of Application Service Data Unit (ASDU) (samples) contained in a sampled value message; i is the number of current quantities contained in each ASDU and u is the number of voltage quantities contained in each ASDU.

The F4000S1I3U3 is a typical SV packet type for protection purposes with 163 bytes and published at a rate of 5216000 bit/s. The sampled values traffic is as background traffic with communication latency much smaller than the protection operating time, i.e. in the order of hundreds of microseconds as compared to a few milliseconds. Consequently, it is not expected that SV latency may affect the protection operation time, and due to this, this traffic is modeled in the ICT simulator as background traffic with no interaction with the Power System simulator.

IV. CO-SIMULATION COORDINATOR SERVER

The different nature of the two simulators as regards simulation time, the PS simulator being time driven while the ICT simulator being event driven, required the development of a specific coordination process, which takes advantage of the time delay consumed in the IED communication board to reduce the frequency of interchanging data between simulators.

The co-simulation control is done in the Co-simulation Coordinator Server, Figure 3. The Coordinator controls the PS simulation time t_{PS} and the ICT simulation time t_{CS} by requesting each simulator to run a defined simulation time span Δt, the co-simulation time step. It acknowledges the completion of the simulation time span by receiving a ready flag from each simulator. When all simulators have completed the requested simulation time span, it requests to run a new simulation time span to all simulators, and the process starts again until the co-simulation reaches the overall time span.

At each simulation time span request, the Coordinator transfers all relevant messages between simulators, i.e. only those whose payload has changed during the previous co-simulation step, as previously explained. The information contained in each message comprehends the IED description where the message lives, payload, GOOSE Identifier (GoID) and the scheduled time. In case the message is transferred from the PS to the ICT simulator, the scheduled time is the instant the message leaves the IED Communication board. In the other way around, the scheduled time is the time instant the message is delivered to the Protection Algorithm.

Examples are presented in TABLES I and II. The GOOSE messages with GoID 201M1G1 and 201M1G2 are published by Device 1 and will be subscribed by Device 2, an outcome of co-simulation time step 1. The publish time is scheduled at 1400 µs for the first message and 1500 µs for the second. This information is transferred from the PS simulator to the ICT simulator at the end of the co-simulation time step, TABLE I.

When the messages finally arrive at Device 2, at the end of co-simulation time step 2, the ICT simulator transfers these messages to the PS simulator, including the time schedule computed by the ICT simulator, for the messages to be delivered to Device 2 Protection Algorithm, see TABLE II.

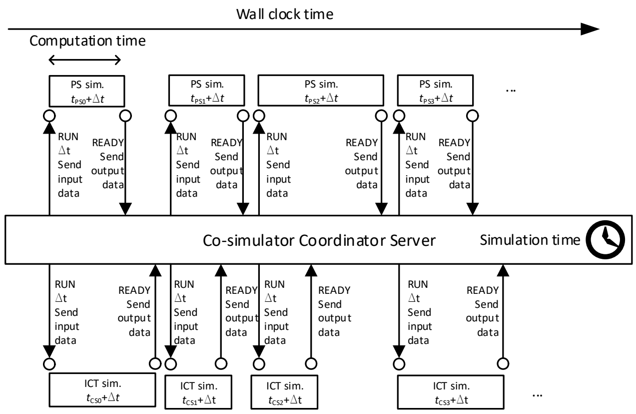

Figure 3. Co-simulation coordination and execution schedule.

TABLE I. MESSAGES FROM PS TO ICT AT THE END OF CO-SIMULATION TIME STEP 1

IED	GoID	Payload	Schedule time (µs)
Device 1	201M1G1	00 00 01 00	1400
Device 1	201M1G2	00 00 02	1500

TABLE II. MESSAGES FROM ICT TO PS AT THE END OF CO-SIMULATION TIME STEP 1

IED	GoID	Payload	Schedule time (µs)
Device 2	201M1G1	00 00 01 00	2463
Device 2	201M1G2	00 00 02	2570

The choice of an adequate co-simulation time step is made recognizing the fact that the PS simulator is time driven while the ICT simulator is event driven. The co-simulation time step should be chosen considering the system time constant. For the PS, this could result in a simulation time step as low as 50 µs for protection scheme studies. For the ICT system, this could be lower than 0.25 µs.

A first approach would be to choose the co-simulation time step equal to the PS simulator time step, e.g., 50 µs. In this case, the IED Protection algorithms will update the GOOSE message payload and receive the messages from the ICT simulator with a resolution of 50 µs, which may be acceptable, since the IED Process and Communication boards processing time is around 1 ms.

The choice of the co-simulation time step must balance the required simulation time resolution and the simulation computation time. Short co-simulation time steps increase the resolution but penalize the computation time. The IED processing time may be used to stretch the co-simulation time step up to 1 ms, without losing simulation time resolution and reducing the computation time. This is better explained in the example presented in Figure 4. Suppose that a certain GOOSE payload is a result of a protection algorithm output in the source IED at 0.4 ms. The IED Processor board sends this payload to the Communication board, which creates the corresponding GOOSE message and delivers to the ICT network, let us suppose after 1 ms, at 1.4 ms. This information is sent from the PS simulator to the ICT simulator that schedules the GOOSE message to be published at 1.4 ms. The ICT simulator computes the GOOSE message latency equal to 63 µs, i.e. the message is delivered at the destination IED Communication board at 1.463

ms. The destination IED will take, let us suppose, 1 ms to unpack the GOOSE payload and will deliver this data to the processor board at 2.463ms. The GOOSE message payload and delivery time are sent from the ICT simulator to the PS simulator, which finally delivers to the protection algorithm at the first simulation time step scheduled time, at 2.500 ms.

As it can be seen, the co-simulation time step can be 1 ms without affecting the simulation results and improve the overall computational time.

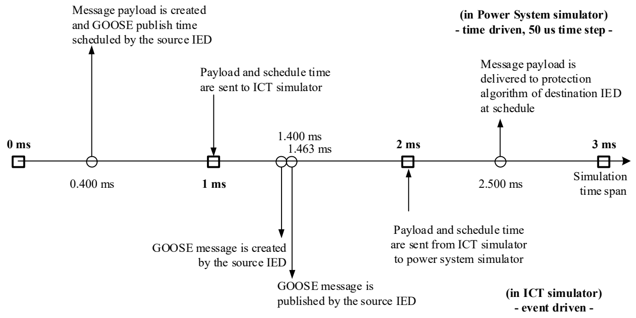

Figure 4. Example of co-simulation exchange data in a stretched co-simulation 1 ms.

V. GOOSE TRAFFIC SEQUENCE DIAGRAM

A GOOSE traffic sequence diagram was developed aiming at showing in a clear manner the GOOSE transmitted and received messages during a simulation.

In the diagram, transmitted GOOSE messages are drawn as horizontal arrows from the publisher IED to the subscriber IED, each arrow is labeled with the GOOSE message identifier and its content. The GOOSE message publishing time is given on both sides of the diagram for readiness. In case the same GOOSE message is subscribed by different IED, subsequent arrows are drawn below the first message, each ending in the corresponding destination IED.

Newly published messages are presented below the previous messages and the time laps are represented by vertical space.

An example of a sequence diagram is presented in Figure 5. IED 1 publishes GOOSE message IED1G1 with content (0 1) at t0 and it is subscribed by IED 2. After that, IED 2 publishes the GOOSE messages IED2G1 with the content (1 1) at t1, which is subscribed by IED 1 and IED 3. Finally, at t2, IED 3 publishes the IED3G1 message with content (0 0 0 0) and subscribed by IED 1.

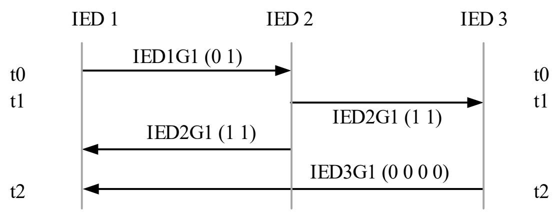

Figure 5. Example of a GOOSE traffic sequence diagram.

VI. APPLICATION EXAMPLE

A. System description

The developed simulation methodology is applied to the protection system of the two bay double busbar with bus coupler station presented in Figure 6. In this example, the feeder in bay 202 is connected to busbar 1, while the feeder in bay 203 is connected to busbar 2. Each bay encompasses one main protection xxxM1, one circuit breaker controller xxxCBC, one merging unit xxxMU1 and one Ethernet switch xxxSW, with xxx being the bay number. At station level, there is a busbar protection 2BBP and one central switch 2SW.

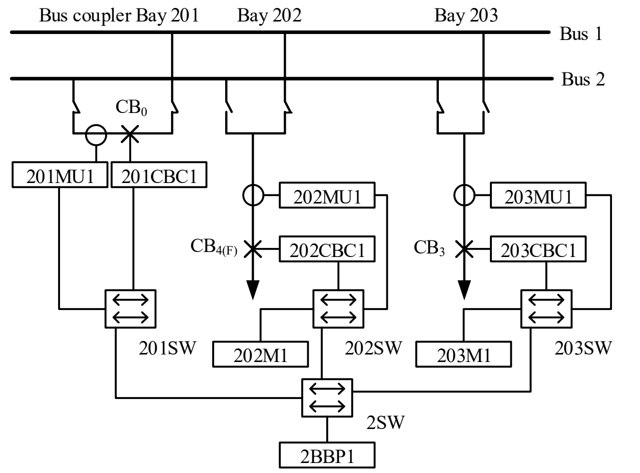

Figure 6. Two bay double busbar with bus coupler station and associated protection system.

The merging units MU are used to measure and publish the analog currents flowing in the bay. The main protection M is used to detect power system faults in the bay feeder and issue a trip command to the associated circuit breaker. The circuit breaker controller CBC, physically commands the CB maneuver and performs the breaker failure function set to operate 100 ms after a trip. Finally, the BBP is used to detect busbar faults and to send trip commands to all necessary CBCs. In case a CBC detects a breaker failure condition, the BBP will also send a trip command to all required IEDs. In this application example, the protection algorithms were modeled with enough detail in order to correctly evaluate the expected generated traffic during a power system fault, i.e. correct modeling of the analog signal processing function and tripping criteria.

When M1 issues a trip command due to a power system fault, it will publish a trip GOOSE message with identifier xxxM1G1 to the CBC1 of the same bay and simultaneously, will publish a xxxM1G2 message (breaker failure start) to the same device. The GOOSE message xxxM1G1 contains 8 bits of data indicating phase A, B and C segregated open/close commands, Trip (01) or Close (10). GOOSE message xxxM1G2 contains 3 bits of data comprehending phase segregated breaker failure start signals.

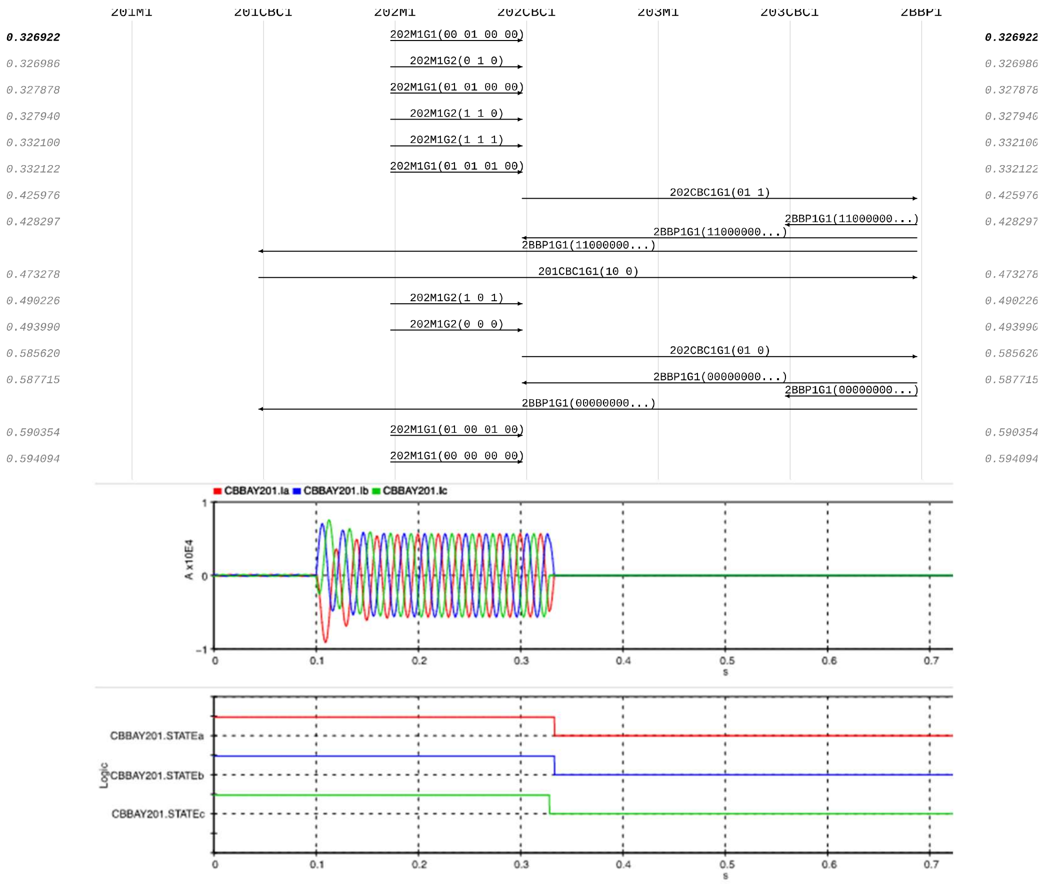

Figure 7. GOOSE Sequence diagram of validation network with breaker failure (top). Bay 201 fault currents and circuit breaker status (bottom). GOOSE sequence diagram and oscillography time references are not the same.

The CBC devices publish the GOOSE message xxxCBC1G1 that contain 3 bits of data indicating the circuit breaker position Open (01) or Close (10) and the circuit breaker failure trip command (1).

The BBP publishes the trip GOOSE message with identifier 2BBP1G1 to all CBC that are associated to the faulty busbar or associated to the busbar to which the failed circuit breaker is connected. The GOOSE message 2BBP1G1 contains a number of bits equal to the number of bays, each bit being a mask for the bay-id to trip.

B. *Power System Fault with Breaker Failure*

At some point in time, a three-phase power system fault occurs in bay 202 leading M1 to start to operate at 0.326922 s. Consequently, it publishes 6 GOOSE messages: 3 circuit breaker open command and 3 breaker failure start messages, according to the pickup phase sequence shown in the GOOSE traffic sequence diagram of Figure 7. Firstly, the protection pickup phase B, followed by phase A and finally phase C. In the same figure, it is presented the buscoupler currents and circuit breaker status.

The 202CBC receives these GOOSE messages, and immediately tries to maneuver the circuit breaker, but unsuccessfully. The 202CBC publishes the breaker failure trip command 202CBC1G1 after 0.09899 s from the reception of the first 202M1G2 GOOSE message to the 2BBP.

The Busbar protection publishes the trip GOOSE message 2BBP1G1 to all 3 CBC but requiring the operation of only the bus coupler and the 202 bay circuit breakers. The buscoupler CBC (201CBC1) receives this request, trips successfully its circuit breaker after 0.14636 s from the 201M1 trip command and reports the new status 201CBC1G1. This extinguishes the fault condition, and subsequently, the drop-off of bay 202 Main device, firstly phase B and finally and simultaneously phase A and C. This, in turn, leads the 202CBC to drop-off the breaker failure trip command, and 2BBP1 informs all bays that the situation is cleared by sending new messages 2BBP1G1.

The event took 267 ms and 15 GOOSE messages were published.

VII. Conclusions

The presented co-simulation architecture was especially developed for studying the performance of protection schemes based on IEC 61850 process bus.

The architecture uses the Co-simulator Coordinator Server to control and synchronize the power system simulators – time driven – and the ICT simulator – event driven. The power system simulator simulates the electrical system and the IEDs protection algorithms, while the ICT simulator simulates the communication network and implements the Ethernet protocol and IEC 61850 communication requirements.

Split modeling of the IEDs is made between the power system and the ICT simulators, based on the processor board and the communication board functional characteristics.

The instances of the GOOSE messages leave the IED communication board scheduled using a uniform random process delay function in the power system simulator. On the other way around, the instances of the GOOSE messages that are delivered to the processor board algorithms are scheduled in the ICT simulator.

The time delay consumed in the IED process and communication boards allows concluding that a 1 ms co-simulation time step is enough to ensure precise simulation results without significantly affecting the overall computational time.

A GOOSE traffic sequence diagram was developed to visually analyze all the generated GOOSE traffic during a power system event. This diagram allows having a perception on the correct operation of complex protection schemes comprehending several IEDs and several publish/subscribe GOOSE messages.

The Co-simulation architecture was implemented in OPAL-RT Hypersim and Riverbed Modeler. A validation scenario was used based on a substation having two feeder bays, each connected to a different busbar and a single buscoupler. The validation scenario was a power system failure in a feeder bay followed by a breaker failure event. Results were presented and analyzed through generated GOOSE traffic sequence diagrams and the fault currents through oscillography.

The developed architecture proved to be adequate for assessing the performance of protection schemes based on process bus, by combining the proven models of native power system simulators with native ICT simulators. It is foreseen that the presented co-simulation method will be extended to other problems including, but not limited to, the assessment of Ethernet time synchronization protocols in process bus networks applied to protection systems or the evaluation of scope extensions to the IEC 61850 standard, for example applications to wide area measurement, protection and control schemes.

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